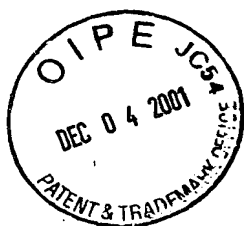


#5/A



PATENTS
Attorney Docket No. 174/183

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

RECEIVED

Applicants : Edward Aung et al. DEC 10 2001
Application No.: 09/805,843 Confirmation Technology Center 2100
Filed : March 13, 2001
For : CLOCK DATA RECOVERY CIRCUITRY ASSOCIATED
WITH PROGRAMMABLE LOGIC DEVICE CIRCUITRY
Group Art Unit : 2182

New York, New York 10020
October 18, 2001

Hon. Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent
application as follows:

12/05/2001 SZEWDIE1 00000082 09805843

In the Claims

01 FC:102 168.00 OP
02 FC:103 360.00 OP

Enter additional claims 102-121 as follows:

102. (New) Programmable serializer circuitry
comprising:

input circuitry that receives a programmable
number of input signals in parallel; and

output circuitry that produces an output
signal that is serially indicative of the input signals one
after another.

103. (New) The circuitry defined in claim 102
wherein the output signal is synchronized with a first clock
signal having a first clock rate, and wherein the circuitry
further comprises:

clock rate divider circuitry that divides the
clock rate by a programmable factor to produce a second
clock signal for timing passage of information indicative of